FE-H Design Organization

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Organization of Basic Tasks:

- What they are and who does them

Status:

- Quick overview of present status

Organization

Basic Tasks for FE-H:

- **Front-end design:** preamplifier and discriminator.
- **Miscellaneous analog cells:** current and voltage DACs, current references, VCCD/VTH amplifiers, FE bias generation cells, LVDS drivers and receivers, and calibration chopper.
- **Control logic:** command decoder, global register, pixel register, pixel control logic, hitbus OR tree, column mask logic, output MUXes.
- **Pixel readout logic:** hit logic, LE/TE RAMs, address ROMs.
- **Bottom of column logic:** sense amplifiers and CEU logic plus buffering.
- **End of column logic:** EOC buffers, horizontal sparse scan, plus buffering.
- **Peripheral digital logic:** grey generator, reset generator, clock generators, self-trigger logic, readout control logic, trigger FIFO, TOT subtractor, serializer.
- **Overall integration and floorplanning**: placing all blocks, routing all interconnects, and assessing global signal distribution issues.

Status Summary:

- First pass of assignments have been made for these tasks.
- TAA agreements are now essentially ready, and we plan to distribute design info.

Status

Overall:

- Layout rules continue to be discussed with Honeywell. We submitted documented list of problems, and have been promised an answer by Nov 30. For now, missing rules in new rule set are replaced by equivalent rules from original rule set.
- Gerrit working on providing Standard Cell library (similar to that of AMS). The intention is to perform higher quality Verilog simulations (including output drive strength), and also to use automatic place and route for non-critical circuit blocks where possible (control logic and digital peripheral logic ?) to accelerate schedule.
- We would like to move to the next major Cadence release (our present 9502 release is no longer supported or distributed by Cadence). The exact sub-version is likely to be 4.4.2. For now we are preparing things in 9502 (4.3.4) because there are conversion utilities to go forward, but not backward.

Front-end Design:

- Laurent has TAA paperwork almost complete. He will spend some time this week with Gerrit to get design information, and begin working on transfer of FE-D front-end design to HSOI in December.

Analog Cells:

- For FE-D, these were designed by Laurent and Peter. There are several new issues to look at, including a CMOS current reference, and a more compact DAC design. In DMILL, there is guaranteed space available under analog power busses. In HSOI (3-metal) this is less attractive, and we need to find space for extra EOC buffers. This work would be shared between Bonn and LBL, depending on manpower and FE-D re-submission in particular. Final validation of these blocks would of course involve Laurent.

Control Logic:

- This was all designed and implemented by Bonn for FE-D, and it is natural that they would do some of this again. We hope to gain by using Synopsys and Gerrit's standard cell library for some of this work, in which case Bonn would only have the custom layout blocks to worry about.

Pixel Readout and CEU Logic:

- Emanuele has begun working on this. He has improved the hit logic in the pixel to eliminate most significant multi-hit problems, and is simulating the column and CEU region using HSOI models and a modified CMOS sense amp design. The next step is to improve the RAM cell design in the pixel.

End of Column Logic:

- No work has begun on this yet. The schematic seems OK, and Mario has done the layout optimization for the present FE-D. He would be a candidate for this work, depending on FE-D resubmission committments.

Peripheral Digital Logic:

- This is being handled by Gerrit, who will discuss progress in a separate talk.

Floorplanning:

- Very little has been done on this yet. There is a preference on the part of some of us for a floor-plan more like that of FE-B, in which the bias and DAC blocks are in the bottom of column region rather than the bottom of the chip. This will evolve as the basic blocks come together.